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LC93913A LM32K10

1. Application

This data sheet is to introduce the Technical Literature LM32K1O, Passive Matrix type LCD Unit.

(320x240 dot, DFST-2, Positive type, with backlight system by cold cathode fluorescent tube (CCFT).]

2. Construction and Outline

Construction: 320x240 full dot graphic display unit

Outline : See Fig. 8,

Connection : See Fig. 8, and Table, 5,

There shall be no scrtches, stains, chips, distortions and other external drawbacks that may affect the display function,

Rejection criteria shall be noted in Inspection Standard S-U-012-01,

2

3. Mechanical Specifications

Table 1

Parameter	Specification		Unit
Outline dimensions	148(W) x 96(HI x 8MAX (D)	Notel	nn
Effective viewing area	100 (W) × 76(H)		mm
Display format	320(W) x 240(H) full dot		
Dot size	0,28(W) x 0.28(H)		mm
Dot spacing	0.02		mm
Character color	Black	Note2	_
Background color	White	Note2	_
Weight	Approx. 140		g ·

Notel: Excluded the mounting tab, (See Fig. 8)

Note2: Due to the characteristics of the LC Material, the colors vary with environmental temperature.

Display Data 'H': Dot on: Black

'L': Dot off: White

4. Absolute Maximum Retings

4-1, Electrical Absolute Maximum Ratings

Table 2

Parameter	Symbol	Min	MAX	Unit	Remark
Supply voltage (Logic)	V _{DD} -V _{ss}	0	6.0	γ	
Supply voltage (LCD Driver)	VDD-VEE	0	28. 5	V	Ta=25°C
Input voltage	YIN	0	VDD	V	
Supply voltage (CCFT)	VCCFT	0	1500	Vrms	
Supply current (CCFT)	ICCFT	0	6.5	mArms	

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4-2. Environmental Condition

Table 3

Item	Tstg	Topr	Remark			
	MIN. MAX.	MIN. MAX.				
Ambient temperature	-25°C +60°C	0" C +45℃				
Humidity	Note 1	Note 1	No condensation			
Vibration	Note 2	Note 2	3 directions (X/Y/2)			
Shock	Note 3	Note 3	6 directions			
			$(\pm X/\pm Y/\pm Z)$			

Note 1) Ta≤40°C··. ···90% RH Max

Ta>40°C······Absolute humidity shall be less than Ta=40°C / 90% RH

Note 2) These test conditions are in accrdance with 'IEC 62-2-6'

Frequency: 10 ~ 55HZ Viblation width: 1.5mm

Interval: $10HZ \sim 55HZ \sim 10HZ$

(1 rein)

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation: 490m/S² (50G)

Pulse width: 11ms

3 times for each direction of $\pm X/\pm Y/\pm Z$.

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5. Electrical Specifications

5.1 Electrical characteristics

Table 4

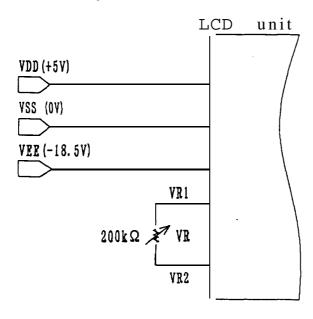
Ta=25°C, $VDD=5V\pm 5$ %

Prameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V _{DD} -V _{SS}		4. 75	5. 0	5. 25	γ
Supply voltage (LCD drive)	Yee-Vss	V _{DD} =5V (Note !)	-19, 0	-18, 5	-18, 0	v
Input signal voltage	VIN	'H'level	0. 8VDD	_	VDD	V
		"L' level	0	-	0. 2VDD	V
Input leakage current	IIL	'R' level			20	μА
		`L' level	-20,0	-	-	μA
Supply current (Logic)	Ipp	$V_{DD}=5V$, $V_{EE}=-18.5V$	Ī	12.5	19	ΔŒ
Supply current (LCD)	Ier	VR=250k Ω		7	10.5	MA
Power consumption (LCD)	PdlCD	F=80HZ (Note 2]	ı	192	288	шW
Start voltage (B/L) (Note.3)	VFTS	Inverter	1000	_	_	Vrms
Supply voltage (B/L)	VFTL	LM000106	225	250	275	Vrms
Supply current (B/L)	IFT	Input voltage 12V	4	5	6	mArms
Power consumption (B/L)	PdFT	adjust resistor	_	1. 25		W
		200kohm				

Note 1] The viewing $angle(\theta)$ where obtains the maximum contrast can be set by adjusting variable resistor between VR1 and VR2. Refer to Fig, 4 for definition of θ .

Note 2) Display high frequency pattern.

Note 3) Start-upuoltage of invertor.





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5-2. Interface signals

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Table 5

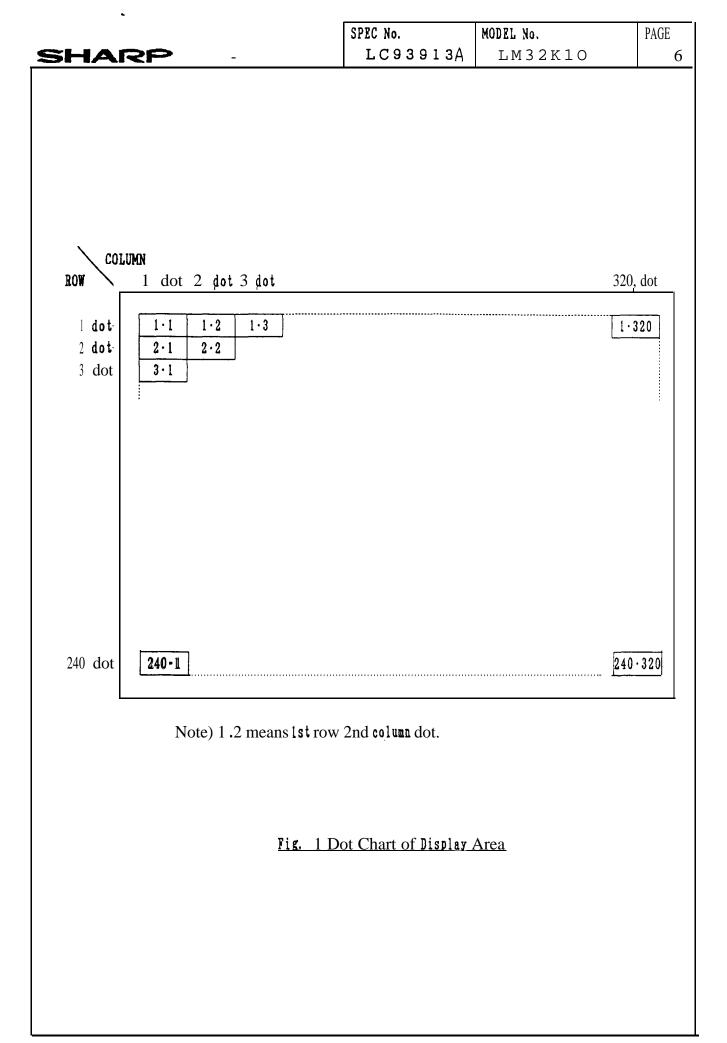
Pin No.	Symbols	Description	Level
1	S	Scan start-up signal	" H "
2	CP1	Input data latch signal	H⇒L
3	CP2	Data input clock signal	H⇒Γ
4	VDD	Power supply for logic and LCD (+5v)	-
5	VSS	Ground potential (GND)	
6	VEE	Power supply for LCD (18.51	
7	DO		
8	Di	Display data signal	H (ON), L (OFF)
9	D2		
10	D3		
11	VR1	LCD Contrast Adjust (A)	
12	VR2	LCD Contrast Adjust (B)	

Used Connector: 52103-1217 [Molex]
Mating Cable: 1.0mm pith, 12pins F. F. C

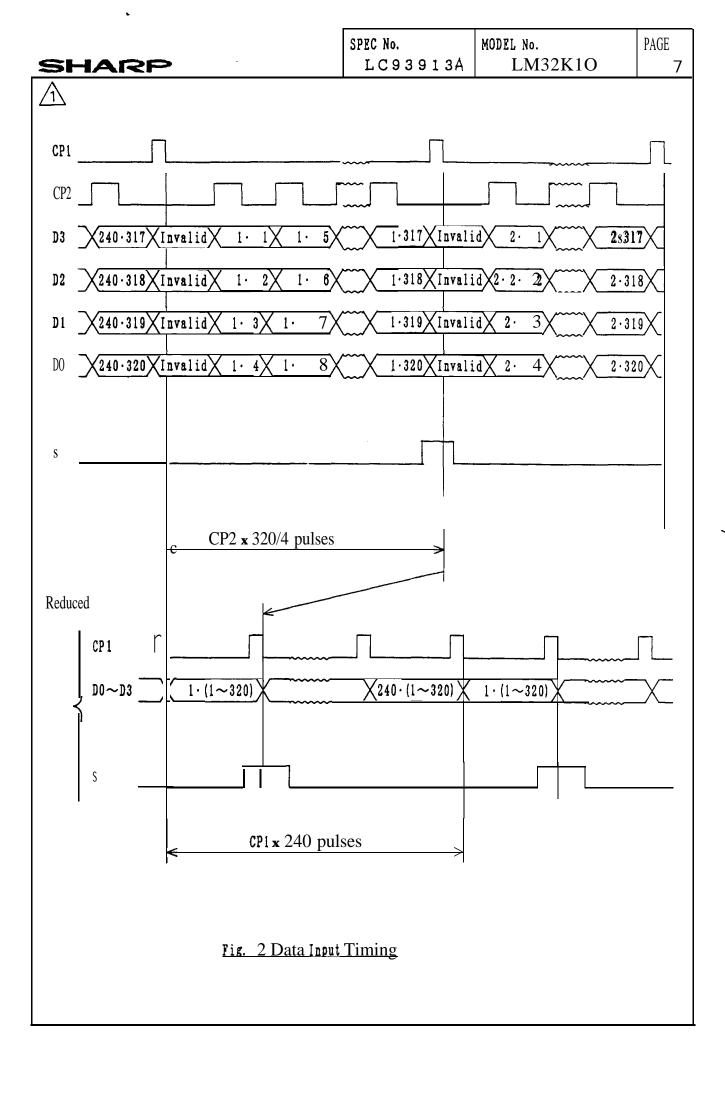
CN2

Pin No.*1	Symbols	Description			
1	VFT 1	Power supply for CCFT back light			
2 V	FT2 Powe	er supply for CCFT back light			

*1: Pin No. and its location are shown in Fig, &.



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SPEC No. MODEL No. PAGE SHARP LC93913A LM32K1O8 tr: | trwH CP 1 TCP2 ts12 CP2 D0~D3 CP2 x (320/4) pulses t_{ssv} S $T_{FRM}=12.5\sim14.3ms$ CP 1 240th first second line's line's line's Reduced data data data transfer transfer transfer S CP1 x 240 pulses VIH=0.8VDD VIL=0.2VDD Fig. 3 Interface Timing Chart

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Table. 8 Interface timing ratings

			Rating			
Item	Symbol	MIN.	TYP.	MAX.	Unit	
Frame cycle	Т им	12.5		14.3	ms	
CP2 clock cycle	Т ср2	152			n s	
'E' level clock width	t cwn	100			n s	
'L' level clock width	t cwr	100			n s	
'H' level latch clock width	t LWH	100		_	n s	
Data set up time	t su	80			n s	
Data hold time	t _{H1}	80			n s	
CP2 ↑ clock allowance time from CP1 ↓	t s12	0			n s	
CP1↑ clock allowance time from CP2↓	t s21	0			n s	
Clock rise/fall time	tr, tf			50	n s	
S Signal Data set up time	t ssu	100			n s	
S Signal Data hold time	t _{sH2}	100			ns	



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6. Unit Driving Method

6-1. Circuit Configuration

Fig. 7 shows the block diagram of the Unit's circuitry,

6-2. Display Face Configuration

The display face electrically consists of signal display segment of 320×240 dots,

6-3. Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits.

Display data which are externally divided into data for each row (320 dots] will be sequentially transferred in the form of 4-bit parallel data through shift resisters by Clock Signal CP2 from the left top of the display face,

When data of one row (320 dots) have been inputted, then lathed in the from of parallel data for 320 lines of signal electrodes by Latch Signal CP1. Then the corresponding drive signal will be transmitted to the 320 lines of column electrodes of the LCD panel by the LCD drive circuits,

At this time, scan start-up signal S has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st rows of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD,

While the 1st rows of data are being displayed, the 2nd rows of data are entered, When 320 dots of data have been transferred then latched on the falling edge of CP1 clock, the display face proceeds to the 2nd rows of display.

Such data input will be repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display by time sharing method, Then data input proceeds to the next display face,

Scan start-up Signal S generates scan signal to drive horizontal electrodes,

The unit shall be driven at the speed of 70~80Hz/frame to avoid flickering.



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Since DC voltage, if applied to LCD panel, causes chemical reaction which will deteriorate LCD panel, drive waveform shall be inverted to prevent the generation of such DC voltage. And to prevent such problem, AC waveform circuit generated by counting CP1 (M generator) is built in this circuit.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit gose up as the operating frequency CP2 increases. Thus the driver LSI applies the system of transferring 4-bit palallel data through the 4 lines of shift resistors to reduce the data transfer speed CP2. Thanks to the LSI, the power consumption of the unit will be minimized,

In this circuit configuration, 4-bit display data shall be therefore inputted to data input pins of $\mathbb{N} \sim \mathbb{N}$ 3.

Furthermore the LCD unit adopts bus line system for data input to minimize the power consumption, In this system data input terminal of each driver LSI is activated only when relevant data input is fed,

Data input for colum electrodes of both the upper and the ower display segment and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20 CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face,

This process is simultaneously followed at the column driver LSI's of both the upper and the lower display segments. Thus data input through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no reflesh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3.

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7. Optical Characteristics

(Table 7 shows the optical characteristics when the viewing angle obtaining the maximum contrast (ϕ) is adjusted to 0- degrees. 1

Table 7			VDD=5V, Ta=25°C					
Parameter	Symbol	Cond	ition	Min.	Typ.	Max.	Unit	Remark
	$\theta_2 - \theta_1$	ø =0°	$C_{o} \ge 2.0$	80	_	_	dgr.	Note 1
	θ 1	$\theta_1 \langle \theta_2$	$C_{o}=2.$ o	-	-	-30	dgr.	Note 1
Viewing angle	θ 2			25	_	_	dgr.	Note 1
range	$\theta_2 - \theta_1$	ø =90°	Co≥2.0	65	_	_	dgr.	Note 1
	θ 1		$C_0 = 2.0$	-	_	-35	dgr.	Note 1
	θ 2	θι(θ2		25	_	-	dgr.	Note 1
Contrast ratio	C。	θ=0°,	ø =0°	8.0	10.0	-		Note 2
Response	τr	$\theta = 0^{\circ}$	ø =0*	_	100	150	ms	Note 3
speed	τd	$\theta = 0^{\circ}$	ø =0°	-	150	200	ms	Note 3

Note 1) The viewing angle range may redefined as shown below,

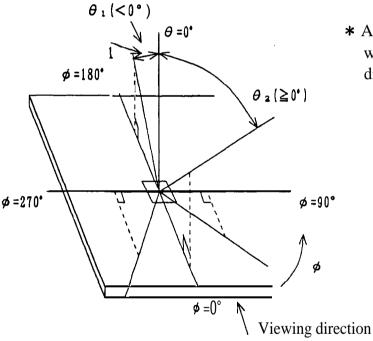


Fig. 4 Definition of Viewing Angle

Note 2) Contrast ratio may be defined as follows:

Contrast ratio is calculated by using the following formula when when the waveform voltage (Fig. 8) is applied in optical characteristics test method (Fig. 5) Photo-detector output voltage with non-select waveform being applied

Photo-detector output voltage with iselect waveform being applied

* Angles θ_1 , θ_2 and ϕ shall fall within the range overwhich the displayed character each be read,

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Note 3) The response characteristics of photo-detector output are measured as shown in Fig. 6, assuming that input signals are applies so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig. 5

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Note 4] Table 7 shown the optical characteristics detected when the LCD applied voltage waveforms are in the highest frequency*.

• The most critics condition for the characteristics of LCD,

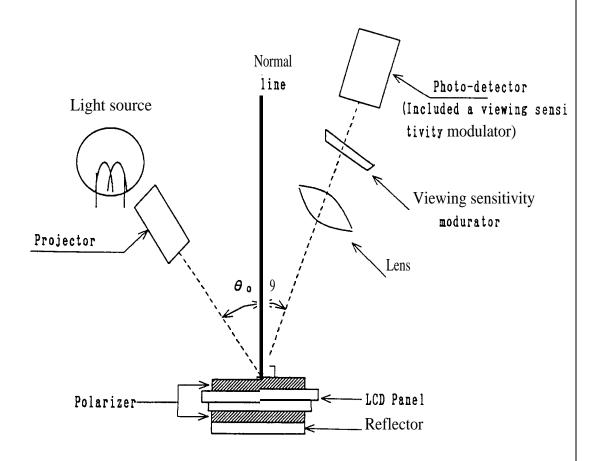


Fig. 5 Optics Characteristics Test Method

SPEC No. MODEL No. PAGE SHARP LC93913A LM32K1O 14 ↑ Drive waveform 1/240 Duty Vo tage applied to LCD cell Non-select waveform Selrct waveform Non-select waveform Response waveform 100% hoto-10% 90% etector utput τd τr: Rise time

Fig. 6 Definition of response Time

τd: Decay time

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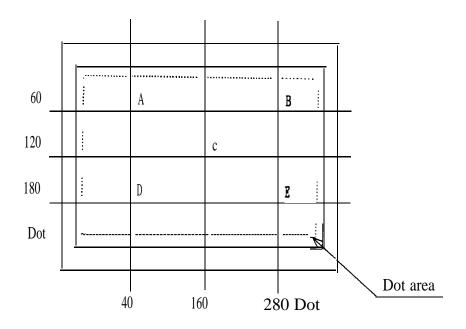
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7-2. Characteristics of Backlightit

(a) Brightness

Parameter	Min.	Typ.	Max,	Unit
Brightness	30	50	-	Cd/m²

Rating are defined as the average brightness at 5 measurement points.



(b) Measurement condition

CCFT inverter: LMOOO106

INPUT voltage: 12,0 IFT: 5mA

LCD unit Condition:

LCD is full dot OFF

VEE=-18.5V

Temperature:

Ta=25°C, 30 minutes after turning on.

Measurement equipment: BM-7 (TOPCON Corporation]

(Cl Operating life time

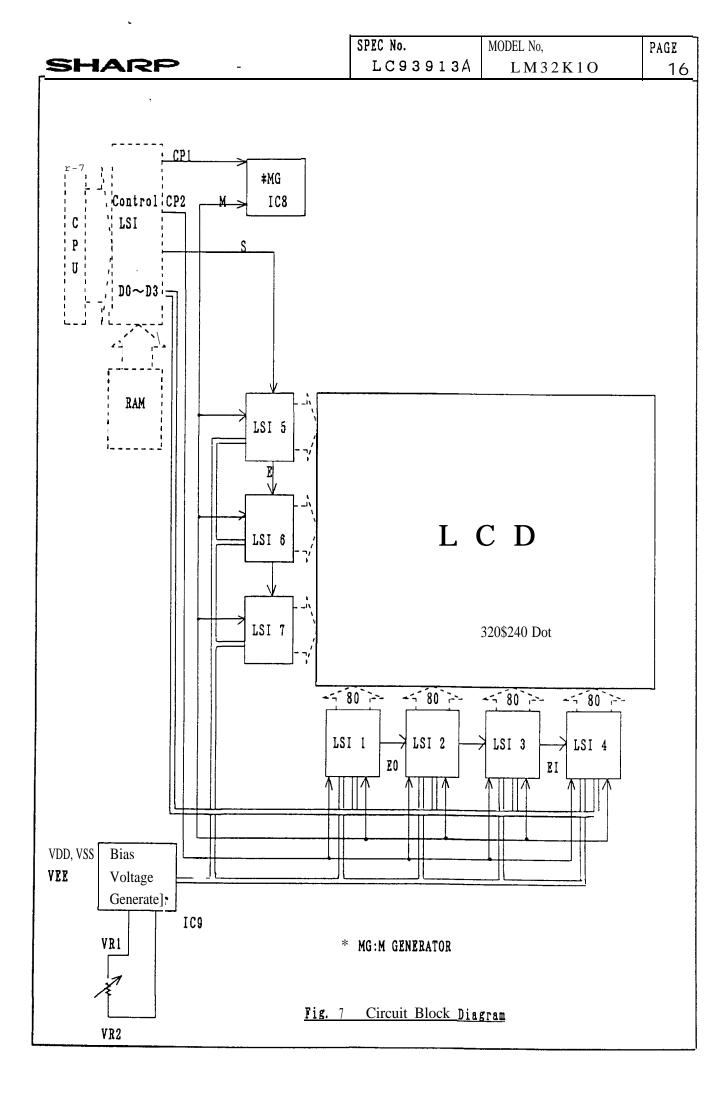
.The oprating life time is 10,000 hours more under the following conditions,

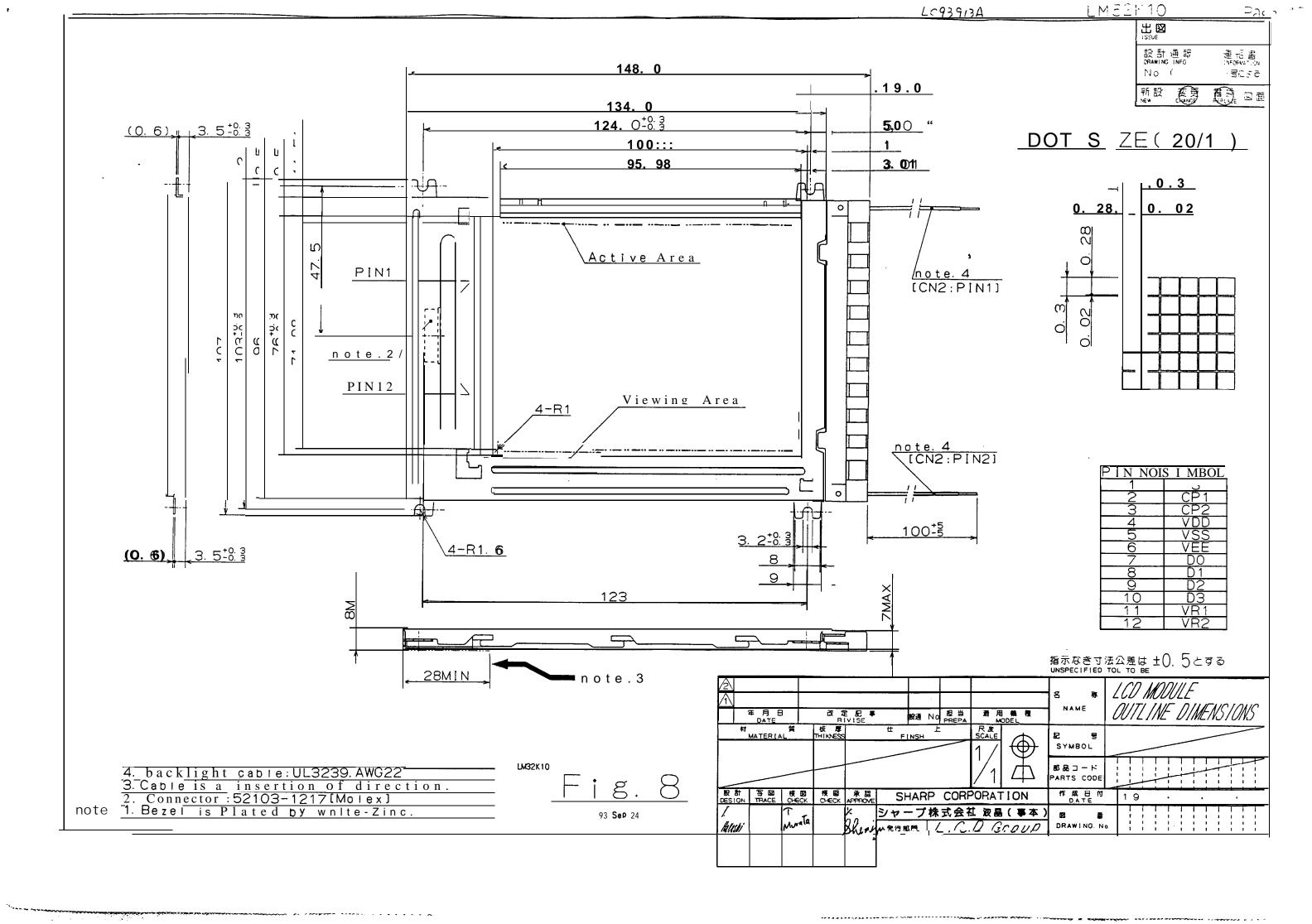
CCFT inverter is

IFT=5mArms

Ta=25 ± 5°C

- The operating life time is defined as having ended when any of the following conditions occur,
 - -When the illuminance or quantity of light has decreased to 50% of the initial value,
 - -When the light of CCFT goes to flicker remarkble.





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8. Precautions

8-1. Angle when installing the unit

This unit's viewing angle is illustrated in Fig. 9.

$$\theta_1$$
 < viewing range < e_2 (e $_1$ < 0° , $\theta_2 \ge 0^{\circ}$)

Please consider the optimum viewing conditions according to the purpose when installing the unit.

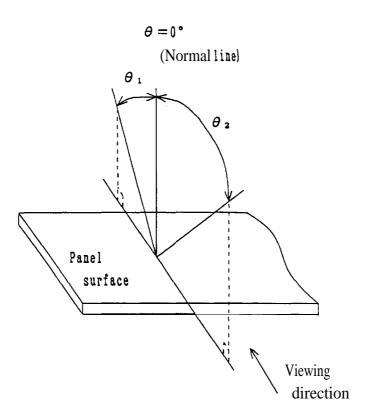


Fig. 9 Dot matrix LCD viewing angle

8-2, Handing cautions

This unit is installed using mounting tabs at the four corners of PCB or bezel,

When installing the unit, pay attention and handle carefully not to allow any undue stress such as twist or bend.

A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.

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8-3. Notes on attachment

- (1) Since the front polarizer is easily dameged, please pay attention not to scratch on its face,
- (2) If the surface of the LCD cells need to be cleaned, wipe it swiftly with cotton or other soft cloth. If still not completely clear, blow on it and wipe,
- (3) Water droplets, etc. must be wiped off immediately since they may cause color changes, stain, etc. if remained for a long time,
- (4) Since LCD is made of glass plates, dropping the unit or banging it against hard objects may cause cracking the or fragmentation,
- (5) CMOS LSIS are equipped in this unit, so care nust be taken to avoid the electro-static charge, by earthing human body, etc. Take the following neasuures, to protect the unit from the electric discharge via mounting tabs from the main system electrified with static electricity.
 - (1) Earth the metallic case of the main system (contact of the unit and main system).
 - (21 Insulate the unit and main system by attaching insulating washers made of backlite or nylon, etc.

8-4, Notes on operation

(1) The unit should be driven according to the specified ratings to avoid malfunction of permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal K.especially the power ON/OFF sequence shown on next page shall be followed to avoid latch-up of driver LSIS and application of DC voltage to LCD page1.

8-5, Others

- (1) Avoid to expose the unit to the direct sun-light, strong ultraviolet light, etc. for a long time.
- (2) If stored at temperatures below specified storage temperature, the LC may fleeze and be deteriorated. If storage temperature exceed the specified rating, the molecular orientation of the LC may charge to that of a liquid, and they may not revert to their original state.
- (3) If the LCD panel is removed from the LCD unit, it may cause the poor contact, So please avoid to dismantle the unit.
- (4) Do'nt use any materials which emit following gas from epoxy resin (amines hardener) and silicon adhesive agent (dealcoholor deoxym) to prevent change polarizer color owing to gas.

SPEC No. MODEL NO. PAGE LC93913A $L\,M\,3\,2\,K\,1\,O$ 2 0 $20 \text{ms} \, \text{MAX}$ ON (5V) O. 8VDD VDD OFF (VSS) í ON (5V) S, CP1, CP2, DATA OFF (VSS) Oms KIN OmasiMIN~ 20msMAX OFF (VSS~VDD) VEE ON (VEE) Oms MIN Oms KIN ON時 OFF時 Fig. 10 Power ON/OFF sequence